REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-11 remain in the application.

In the section entitled "Claim Rejections - 35 USC § 102" on pages 2-4 of the above-mentioned Office action, claims 1-3, 5, 7-8, 10-11 have been rejected as being anticipated by Dähn (US 6,539,505 B1) under 35 U.S.C. § 102(b).

In the section entitled "Claim Rejections - 35 USC § 103" on pages 4-7 of the above-mentioned Office action, claims 4, 6, and 9 have been rejected as being unpatentable over Dähn in view of Morgan et al. (US 6,072,737) under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> a data change circuit connected between said data input line and the memory circuit, said data change circuit being controllable depending on a result of a comparison performed in said comparator unit such that when an error occurs, further test data can be written to the memory circuit in a manner altered by said data change circuit.

Claim 7 calls for, inter alia:

> transmitting further test data after a detection of the error, the further test data being altered during writing to the memory area resulting in altered test data being written into the memory area such that a subsequent comparison of the altered test data read out and the further test data yields a difference.

The invention of the instant application relates to a test circuit for testing a memory circuit (13) which includes a date input line (10) for providing test data to be written to the memory circuit, a comparator unit (12) connected to the data input line and to the memory circuit wherein the comparator unit compares expected values received over the data input line (10) with the test data read from the memory circuit (13), the test data previously having been written to the memory circuit over the data input line, and a data change circuit (15) connected between the data input line and the memory circuit, wherein the data change circuit is controllable depending on a result of a comparison performed in the comparator unit such that when an error occurs, further test data can be written to the memory circuit in a manner altered by the data change circuit.

One concept of the invention of the instant application is that a number of memory tests can be performed without reading out test result data. In particular, in case of soft error it can occur that an error in a memory cell is detected in one test process and not detected in a following test process. Therefore, conventionally, after each test process test results have to be read out by a tester unit. According to the invention of the instant application, it is not provided that a test process is carried out to test the memory circuit wherein if an error occurs it is provided in a next test process the data which are written in the respective memory cell of the memory circuit are modified such that a following comparison of the written and read out data results in the detection of an error even if the respective memory cell has stored the written data in the following test process correctly. The invention of the instant application allows to carry out a plurality of test processes in the memory circuit without instantaneously reading out the test results and without losing any Information about the occurrence of soft errors detected in any of the test processes.

Dähn shows a test circuit for testing one bank of a memory circuit wherein the test result is stored in other banks of the memory circuit. Therefore, a bit fall map is stored in not tested areas (banks) such that plurality of test processes

can be performed with the bank to be tested and the respective test results can be used for updating each of the copies of the bit fail map in the other memory banks. The test circuit includes a comparator unit which compares expected values received over a data input line with test data read out from the memory circuit. A test result is determined by comparing the data value read out and the desired value written in. A changeover device is provided which is connected to each of the memory banks wherein the changeover device has a multiplexer having an input and an output and a de-multiplexer having an input and an output, wherein the changeover device is connected to receive a respective address for selecting a memory bank, a terminal for a data signal of the memory bank connected to the output of the multiplexer and the input of the de-multiplexer wherein the input of the multiplexer and the output of the multiplexer are connected to a signal line for the predetermined data value to be stored and the data value to be read out subsequently and to a signal line for a data value for the comparison result to be written and to be read out subsequently.

The test circuit according to Dähn does not include a data change circuit according to the invention of the instant application. Dähn does not show a data change circuit, which is connected in the data input line and which is able to

change the test data value written into the memory circuit depending on a result of a comparison performed in a proceeding test process. In other words, the changeover device according to Dähn does nothing more than copying the comparison result into each of the memory banks not being tested therefore does not change any test data to be written into the memory bank to be tested. Moreover, the changeover device of Dähn has no functionality, which depends on a result of the comparison performed in the comparator unit since the comparison results are copied into the memory banks not being tested, i.e. in case of an error and in case of no error.

Claims 1 and 7 are, therefore, believed to be patentable over Dähn and since all of the dependent claims are ultimately dependent on claims 1 or 7, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-11 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

Yonghong Chen
Reg. No. 56,150

For Applicants

YC

March 27, 2006

Lerner Greenberg Stemer LLP
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101